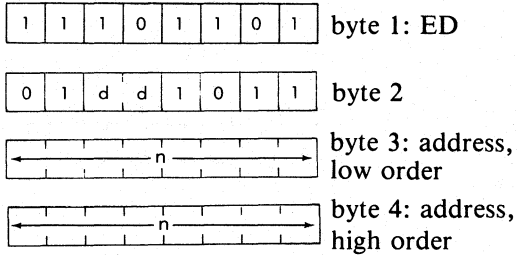## LD dd, (nn)

Load register pair dd from memory locations addressed by nn.

Function:

$$dd_{low} \leftarrow (nn); dd_{high} \leftarrow (nn+1)$$

Format:

| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | byte 1: ED

| 0 | 1 | d | d | 1 | 0 | 1 | 1 | byte 2

| ← n → | byte 3: address, low order
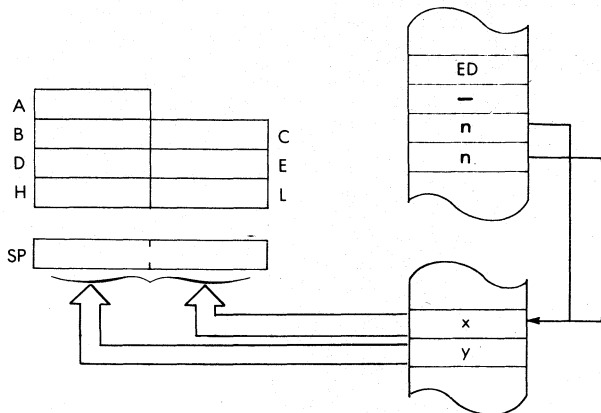
| ← n → | byte 4: address, high order

Description:

The contents of the memory location addressed by the memory locations immediately following the opcode are loaded into the low order of the specified register pair. The contents of the memory location immediately following the one previously loaded are then loaded into the high order of the register pair. The low order byte of the nn address immediately follows the opcode. dd may be any one of:

BC – 00	HL – 10
DE – 01	SP – 11

Data Flow:

Timing: 6 M cycles; 20 T states; 10 usec @ 2 MHz

Addressing Mode: Direct.

Byte Codes:
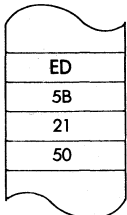
d'd: BC DE HL SP
ED- | 4B | 5B | 6B | 7B |

Flags:

S   Z   H   P/V N   C

| | | | | | | | | **(no effect)**

Example: LD   DE, (5021)

Before: After:

D[DBE2   ]E   D[///////30F4///////]E

| ED |
| 5B |
| 21 |
| 50 |

OBJECT CODE

| 5021 | F4 |
| 5022 | 30 |

| 5021 | F4 |
| 5022 | 30 |