THE Z80 INSTRUCTION SET

E9

Description:	The contents of the HL register pair are loaded into the program counter. The next instruction is
	fetched from this new address.
Data Flow:	
	A B C E
	4 7 7 7
	PC (
Timing:	1 M cycle; 4 T states; 2 usec @ 2 MHz
Addressing Mod	de: Implicit.
Flags:	S Z H P/V N C (no effect).
Example:	JP (HL)
	Before: After:
	H 0411 L H 0411 L
E9	PC B001 PC
OBJECT CODE	

Jump to HL.

PC ← HL

JP (HL)

Function:

Format: