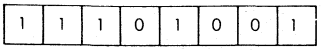
JP (HL) Jump to HL.

Function: PC ← HL

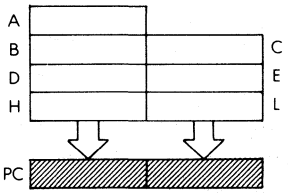
Format:



E9

Description: The contents of the HL register pair are loaded into the program counter. The next instruction is fetched from this new address.

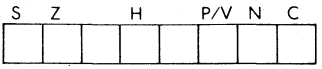
Data Flow:



Timing: 1 M cycle; 4 T states; 2 usec @ 2 MHz

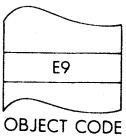
Addressing Mode: Implicit.

Flags:

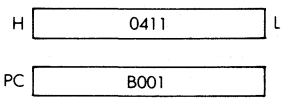


(no effect).

Example: JP (HL)



Before:



After: