CPIR

Block compare with increment.

Function:

A — [HL]; HL ← HL + 1; BC ← BC — 1;
Repeat until BC = 0 or A = [HL]

| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | byte 1: ED

| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | byte 2: B1

Description:

The contents of the memory location addressed by the HL register pair are subtracted from the contents of the accumulator and the result is discarded. Then the HL register pair is incremented and the BC register pair is decremented. If BC ≠ 0 and A ≠ [HL], then the program counter is decremented by 2 and the instruction is re-executed.

Data Flow:
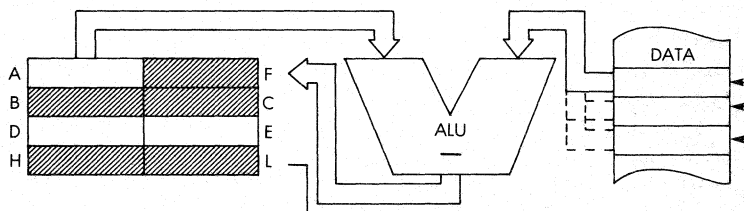
Timing:
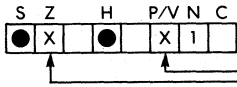
BC = 0 or A = [HL] : 4 M cycles; 16 T states: 8 usec @ 2 MHz
BC ≠ 0 and A ≠ [HL] : 5 M cycles; 21 T states: 10.5 usec @ 2 MHz

Addressing Mode: indirect.

Flags:

S   Z   H   P/V N C

● X   ●   X 1

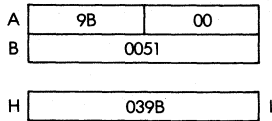*Reset if BC* = 0 after execution; set otherwise
Set if A = [HL]

Example: **CPIR**

Before: After:

A	9B	00
B	0051	

A | 9B | 46
B | 004F |

H | 039B | L

H | 039D | L

ED	
B1	

OBJECT CODE

039B	2A
039C	9B
039D	06

039B	2A
039C	9B
039D	06