CPDR

Block compare with decrement.

Function:

A — [HL]; HL ← HL — 1; BC ← BC — 1;
Repeat until BC = 0 or A = [HL]

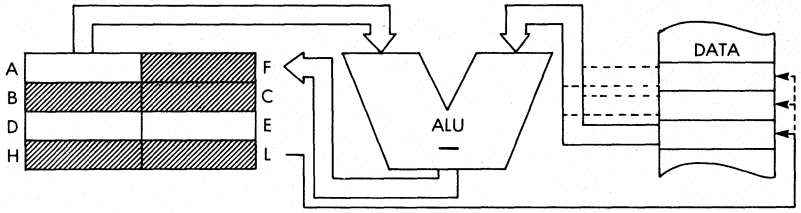
Format:

1	1	1	0	1	1	0	1	byte 1: ED
1	0	1	1	1	0	0	1	byte 2: B9

Description:

The contents of the memory location addressed by the HL register pair are subtracted from the contents of the accumulator and the result is discarded. Then both the BC register pair and the HL register pair are decremented. If BC ≠ 0 and A ≠ [HL], the program counter is decremented by two and the instruction is re-executed.

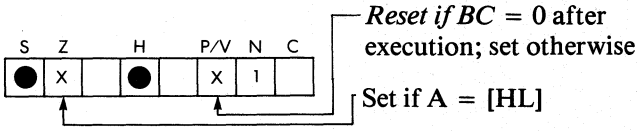
Data Flow:



Timing:

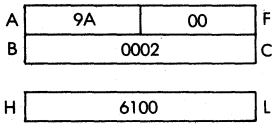
BC = 0 or A = [HL]: 4 M cycles; 16 T states: 8 usec @ 2 MHz
BC ≠ 0 and A ≠ [HL]: 5 M cycles; 21 T states: 10.5 usec @ 2 MHz

Flags:



Example: CPDR

Before:



After: