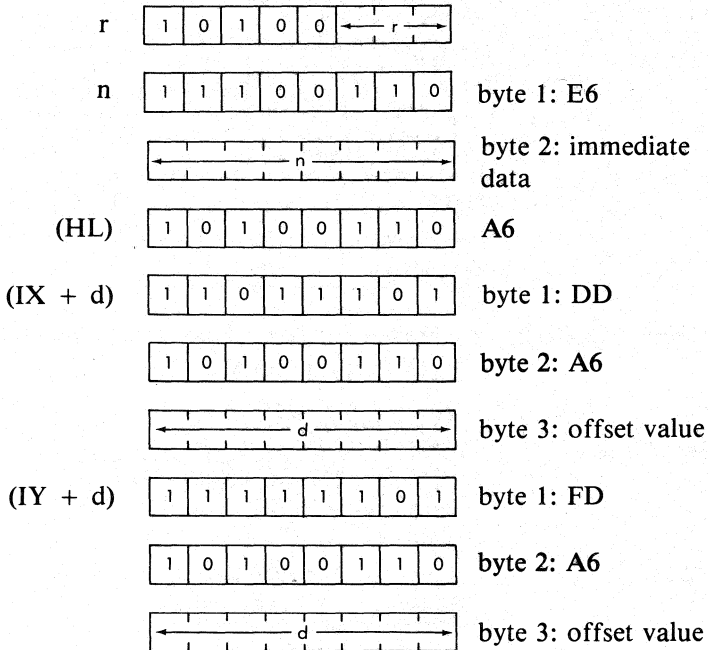


THE Z80 INSTRUCTION SET

AND s Logical AND accumulator with operand s.

Function: $A \leftarrow A \wedge s$

Format: s: may be r, n, (HL), (IX + d), or (IY + d)



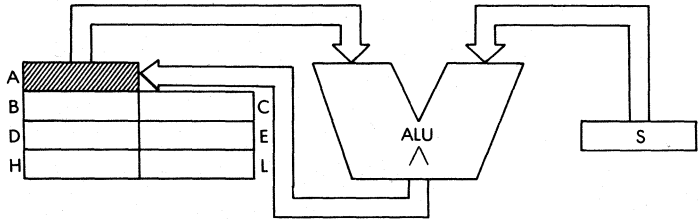
r may be any one of:

A - 111	E - 011
B - 000	H - 100
C - 001	L - 101
D - 010	

Description: The accumulator and the specified operand are logically 'and'ed and the result is stored in the accumulator. s is defined in the description of the similar ADD instructions.

PROGRAMMING THE Z80

Data Flow:



Timing:

<i>s:</i>	<i>M cycles:</i>	<i>T states:</i>	<i>usec @ 2 MHz:</i>
r	1	4	2
n	2	7	3.5
(HL)	2	7	3.5
(IX + d)	5	19	9.5
(IY + d)	5	19	9.5

Addressing Mode: r: implicit; n: immediate; (HL): indirect; (IX + d), (IY + d): indexed.

Byte Codes:

AND r

r: A	B	C	D	E	H	L
A7	A0	A1	A2	A3	A4	A5

Flags:

S	Z		H	Ⓟ	V	N	C
●	●		1	●	○	○	

Example:

AND 4B

Before:

A 36

After:

A 02

